Main Features of Polar-ITP IP Core

- An FPGA based polar encoder and decoder integrated test platform (Polar-ITP) IP Core was developed for precise communication performance measurement of polar codes up to 100 Gb/s throughput.
- Polar-ITP supports polar non-systematic and systematic encoders and three types of polar decoders: Successive Cancellation (SC), Majority Logic aided SC (SC-MJL) and SC with list (SC-List) decoders.
- The polar decoders in Polar-ITP IP Core employ fully-parallel and unrolled hardware architecture with dedicated processing elements for each set of block length and code rate.
- The resource utilization of Polar-ITP was optimized using adaptive quantization of log-likelihood ratios (LLRs) and register balancing techniques for the pipelined processing stages.
- The real-time FPGA tests enable an accurate measurement of 10^{-15} bit error rate (BER) and 10^{-12} frame error rate (FER).
- The net coding gain of Polar (1024, 854) SC-MJL decoder is approximately measured as 6.5 dB at 10^{-15} BER.
- The target FPGA of Polar-ITP IP Core is the Xilinx Virtex Ultrascale+ (xcvu9p-flgb2104-2-i) provided by Amazon Web Services (AWS) on f1.2xlarge instance.

General Description of Polar-ITP

The flowchart of the Polar-ITP is illustrated in Figure 1.

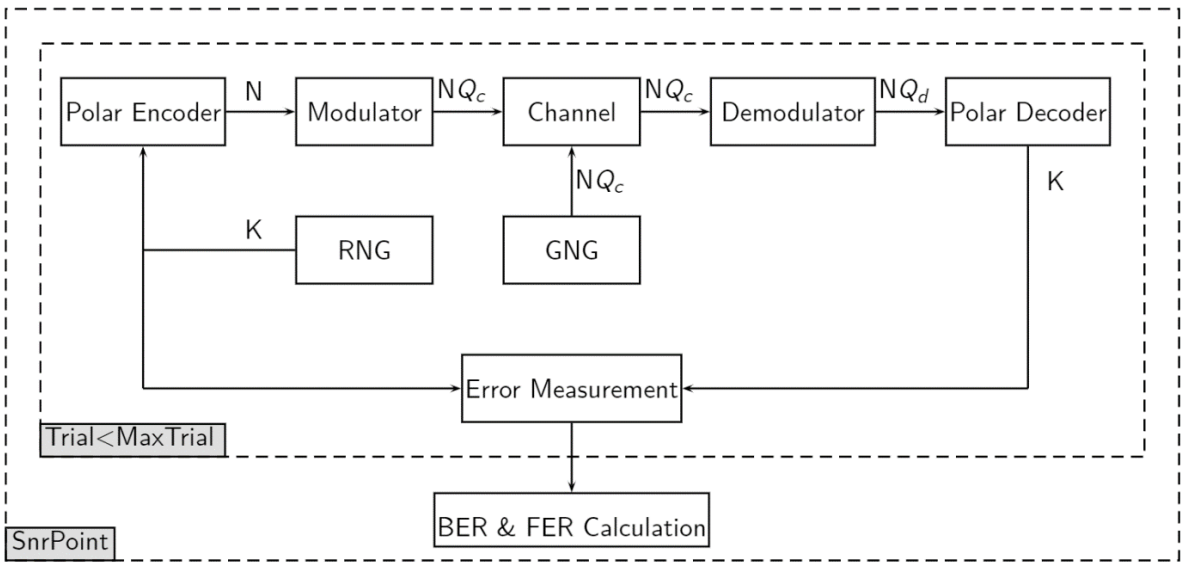

Figure 1: Flowchart of the Polar-ITP where K is the payload, N is the block length, Q_c is the channel bit precision, Q_d is decoder input precision in bits respectively.

The working principle of Polar-ITP is as follows. Initially, an LFSR based Random Number Generator (RNG) generates K pseudo-random information bits. These bits are encoded by Polar Encoder to generate a valid polar codeword. If the user selects non-systematic mode, the codeword includes only parity bits; otherwise, both systematic bits and parity bits are available. Then, the Modulator takes N bits input from the Polar Encoder module and maps the encoded bits to the +1 and -1 symbols using binary phase shift keying (BPSK) modulation, where each symbol has Q_c bit precision. The Channel module combines the symbols and channel noise, which is generated from Gaussian Number Generator (GNG) module. GNG module generates N Gaussian pseudo-random value each having 16 bits precision.

The second half of the Polar-ITP starts with the demodulator module. The Demodulator transforms the channel output to LLRs, each having Q_d bit precision. After that, Polar Decoder module receives LLRs and calculates an estimate of the transmitted information sequence. The Error Measurement module compares the estimated information sequence with the original sequence and calculates the BER and FER of the target polar code.

The dashed lines on the data flowchart represent the “for” loops for each number of trials and Eb/No values. For an inner loop iteration, the number of trials is incremented by one. After the maximum number of trials or frame errors has been reached, the Polar-ITP has forced soft reset to all submodules and initiates with a new Eb/No value.

Input and Output Ports of Polar-ITP

The general description of the I/O ports of the Polar-ITP module is shown in Table 1.

Table 1: I/O ports of the polar-ITP.

Port Name	Sense	Port Width (bits)	Description
CLK	Input	1	***Clock.*** All synchronous logic operations are triggered by rising edge of CLK.
RESET	Input	1	***Reset.*** Synchronous reset for initialization.
MAX_FEN	Input	20	***Maximum frame error.*** Number of maximum frame errors allowed for each member of EBN0 array.
SELECT_EBNO	Input	6	***Selected Eb/No for data display.*** The results are displayed according to this input value. For example, if SELECT_EBNO is 0, the TRIAL, FEN and BEN results for the first Eb/No record will be displayed at the output ports.
TRIAL	Output	50	***Number of trials.*** Current number of trials.
FEN	Output	20	***Number of frame errors.*** Current number of frame errors.

BEN	Output	20	***Number of bit errors.*** Current number of bit errors.
PREC_DEC	Constant	Q_d	***Decoder precision.*** Demodulated data will be represented with Q_d bits.
PREC_CHAN	Constant	Q_c	***Channel precision.*** Modulated data will be represented with Q_c bits.
EBN0	Constant Array	63 x 11	***Eb/No array.*** A record of SNR points to be simulated.

Further information about I/O ports is as follows.

- The CLK port is connected to MMCM or PLL clocking resource of the target FPGA.
- All input ports are connected to a Virtual Input Output (VIO) IP core.
- All I/O ports are connected to Integrated Logic Analyzer (ILA) IP core.

Communication Performance of Polar-ITP IP Core

The BER versus Eb/No performance of the Polar-ITP is depicted in Figure 2. The block length equals to 1024 bits, the payload is 854 bits and Q_d is 5 bits and the type of the polar decoder is SC-MJL. Note that EbNo array ranges from 2 to 8.5 dB with 0.5 dB step size. Each member of EbNo array is simulated with the same initial seed for RNG and GNG modules. The measurements show that the coding gain is approximately 6.5 dB at 10^{-15} BER.

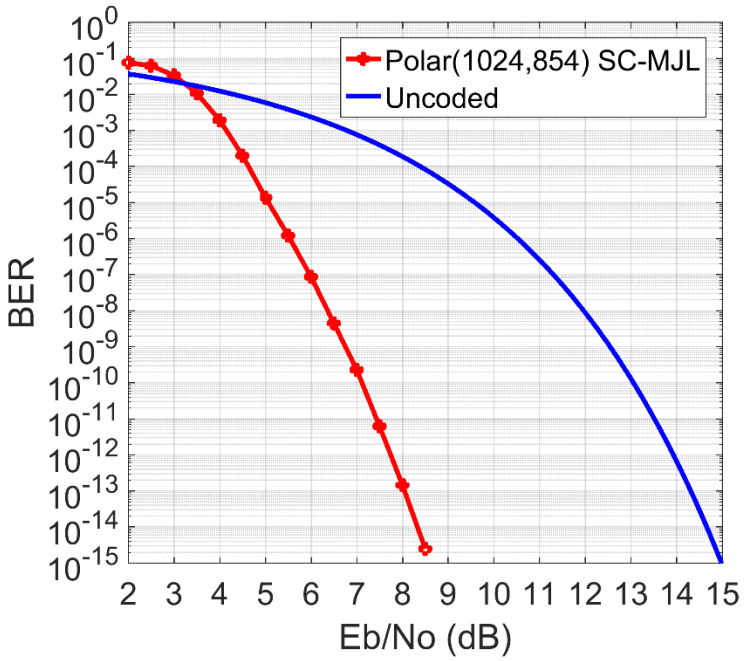

Figure 2: Communications performance and coding gain with respect to uncoded transmission of a polar code with block length equals to 1024 bits, payload equals to 854 bits and Q_d equals to 5 bits under SC-MJL decoding algorithm, AWGN channel and BPSK modulation.

FPGA Implementation Results

The resource utilization of Polar-ITP on Xilinx Virtex Ultrascale+ FPGA is shown in Table 2 and Table 3. The Polar-ITP has 66.1 percent Configurable Logic Block (CLB) of the target FPGA. The frequency of Polar-ITP is 125 MHz, which supports 104 Gb/s information bit throughput at the output of polar decoder. Due to the massive parallelization of data processing, the most complex module in Polar-ITP is the AWGN Channel (combination of Channel and GNG), which utilizes 21.5 percent CLB LUTs of the whole FPGA. The resource utilizations of polar encoder and decoder are remarkably low due to the unrolled and fully-pipelined architecture with advanced quantization and register balancing techniques.

Table 2: Resource utilization of Polar-ITP on Xilinx Virtex Ultrascale+ FPGA

Name \ Resources	CLB LUTs	CLB Registers	CLB	BRAM	URAM	DSP
Capacity of the Target FPGA	1181768	2363536	147721	2160	960	6840
AWS Total Utilization	479322	679620	97680	1383.5	43	3075
Polar-ITP	323430	465454	65283	1175	0	3072
Encoder (Comb.)	1839	1880	1049	0	0	0
Decoder (SC-MJL)	57730	36184	10546	136	0	0
AWGN Channel	253667	412767	53300	1024	0	3072

Table 3: Resource utilization percent of Polar-ITP on Xilinx Virtex Ultrascale+ FPGA

Name \ Resources	CLB LUTs	CLB Registers	CLB	BRAM	URAM	DSP
AWS Total Utilization	40.6	28.8	66.1	64.1	4.5	45.0
Polar-ITP	27.4	19.7	44.2	54.4	0.0	44.9
Encoder (Comb.)	0.2	0.1	0.7	0.0	0.0	0.0
Decoder (SC-MJL)	4.9	1.5	7.1	6.3	0.0	0.0
AWGN Channel	21.5	17.5	36.1	47.4	0.0	44.9

Document Changelog

Version	Publish Date	Changed Content/Page	Reason
0.1	04.03.2019	Document Template	The first template was written.
1.0	08.03.2019	Recent implementation results were included.	An update for the newer implementation results.
1.1	13.05.2019	Whole document.	Typos were corrected.

For more detailed information, please send an email to info@polaran.com.

We may provide the following inputs to our customers:

- Polar code structure and the indicator vector of the frozen/free bits.
- A replica of the HDL polar decoder in software to perform fixed-point simulation and verification.
- Testbench and test-vectors.
- Detailed behavioral documentation of the polar decoder.