Features

- Verified on Xilinx FPGAs (Kintex-7, Virtex-7 Ultrascale+).
- Meet Cloud Radio Access Network (C-RAN) fronthaul requirements in terms of high data throughput, low latency and low energy consumption.
- Implements unrolled and pipelined decoding architecture with dedicated processing units.
- Adjustable generic I/O port size with respect to code block length (N), code rate (R) and payload (K).
- Supports R=
$$\begin{cases} \left(\frac{1}{2},\frac{3}{4},\frac{4}{5},\frac{5}{6},\frac{15}{16}\right) & for\ N = 1024 \\ \left(\frac{5}{6},\frac{15}{16}\right) & for\ \ N = 2048 \\ \left(\frac{5}{6}\right) & for\ \ N = 8192 \end{cases}$$
- In addition to the predefined code rates, other code rates can be supported on demand.
- Supports 100 Gb/s data speed, and more than 7.5dB coding gain.
- Compatible with Xilinx Vivado versions greater than 2016.1.

General Description

The PD-100G is designed for C-RAN fronthaul to decode In-phase and Quadrature components of the signal transmitted from Remote Radio Heads (RRH) to Baseband Unit (BBU) Pool through optical links. The decoder satisfies the low latency and high throughput requirements of the optical link between RRH and BBU. The throughput of the decoder achieved 100 Gb/s for the provided design configurations.

The decoder is compatible with the PE-100G polar encoder IP core product of POLARAN. PD-100G is a fully parallel pipelined decoder. It can accept input data from “data_in” port at each rising edge of clock, when the “data_en” port is high. After decoding is completed, the “valid” port will be ‘1’ and the decoded bits are available at the “data_out” port.

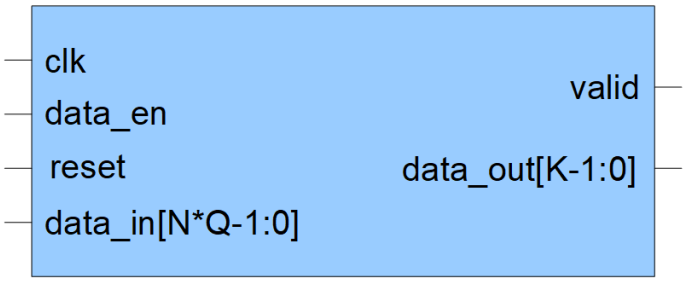

Figure 1: Block Diagram of PD-100G

Input/Output Ports

The descriptions of I/O ports of the PD-100G are stated in Table 1.

Table 1: I/O Ports

Pin	Sense	Port Width (bits)	Description
CLK	Input	1	***Clock.*** All synchronous logic operations are triggered by rising edge of CLK.
DATA_IN	Input	NQ	***Input Data.*** LLR data are given to the decoder through this port. The port width of the encoded data is N.
DATA_EN	Input	1	***Data Enable.*** Marks the valid input data.
DATA_OUT	Output	K	***Output Data.*** Consists of decoded information bits.
VALID	Output	1	***Valid Output Data.*** Marks the valid output data.
PREC	Generic	Q	***Precision.*** Encoded data will be represented with Q bits.

Further explanations about I/O ports are shown below.

Clock (CLK)

All synchronous logic operations of the system are triggered by rising edge of the CLK signal.

Data Enable (DATA_EN)

The active high DATA_EN signal marks the valid input data at the applied to DATA_IN port.

Input Data (DATA_IN)

The decoder accepts input data from DATA_IN port. The input data consists of the channel output in the form of LLR.

Output Data (DATA_OUT)

The decoded information bits are available in the DATA_OUT port when VALID is high. The data width of the DATA_OUT port is ‘K’, which is the number of information bits.

Valid (VALID)

When the output data at the DATA_OUT port is available, the active high. VALID signal becomes ‘1’. Otherwise, VALID is ‘0’.

Precision (PREC)

Each LLR value at the input is represented by PREC number of bits.

Detailed Information of PD-100G

PD-100G is implemented on Kintex-7 and Virtex-7 Ultrascale+ Xilinx FPGAs. The implementation results are shown in Table 2.

Table 2: FPGA Implementation Results of the PD-100G Polar Decoder

FPGA Type	Block Length	Coding Rate	Frequency (MHz)	Throughput (Gb/s)	LUT (K)	FF (K)	BRAM
Kintex-7 (xc7k325t)	1024	1/2	120	61.44	104	58	172
		3/4		92.16	90	53	172
		4/5		98.30	103	61	172
		5/6		102.48	96	57	172
		15/16		115.20	61	38	129
Virtex-7 Ultrascale+ (xcvu9p)	2048	5/6	60	102.48	213	115	471
		15/16		115.20	166	86	279
	8192	5/6	25	170.68	642	393	1539

The communication performance results are shown in Figure 5.

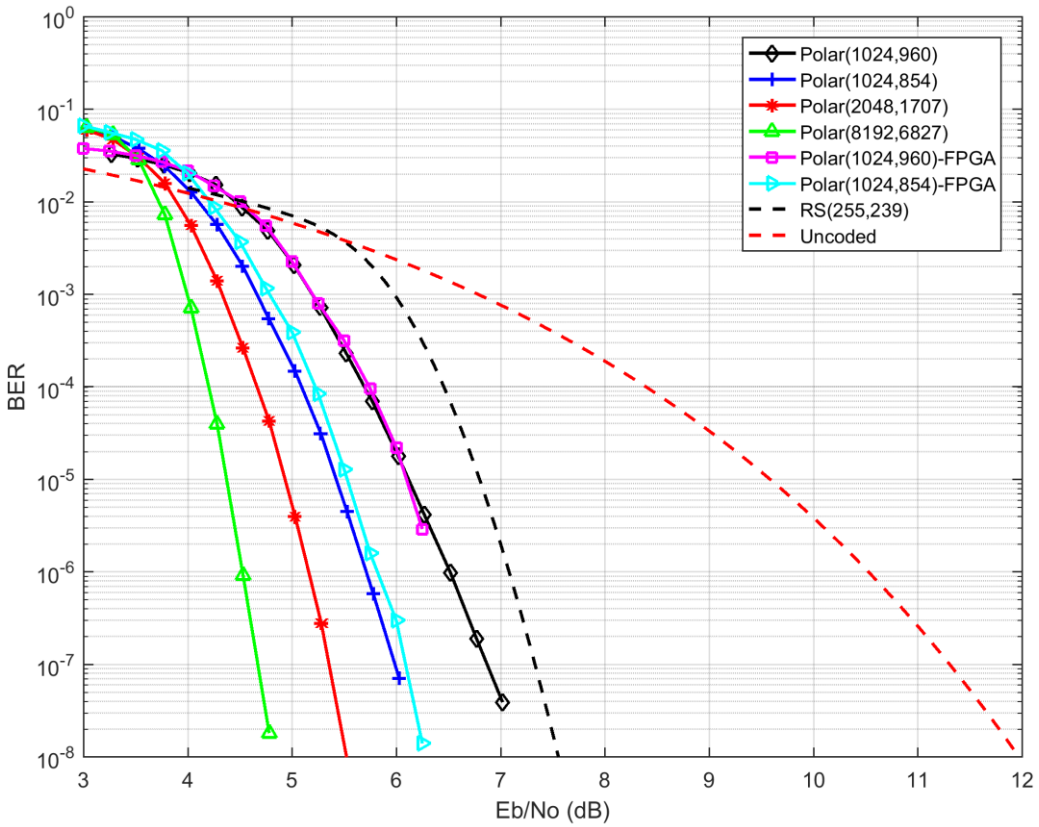

Figure 5: BER performances of the PD-100G family

Document Changelog

Version	Publish Date	Changed Content/Page	Reason
1.0	30.01.2018	Whole document	First version of this document was written.
1.1	24.07.2018	New designs are added, resource usage was updated.	New results.
1.2	13.05.2019	Results were updated.	New results.

For further information, please send an email to info@polaran.com.

We may provide the following inputs to our customers:

- Polar code structure and the indicator vector of the frozen/free bits.
- A replica of the HDL polar decoder in software to perform fixed-point simulation and verification.
- Testbench and test-vectors.
- Detailed behavioral documentation of the polar decoder.