Product Brief

Polar Decoder PD-HL 1.1

Main Features

- Implements the successive cancellation hybrid list decoding algorithm for polar codes
- Drop-in IP core
- Supports data rates in hundreds of Mb/s on standard FPGAs

General Description

Block diagram of PD-HL 1.1 is shown in Fig. 1.

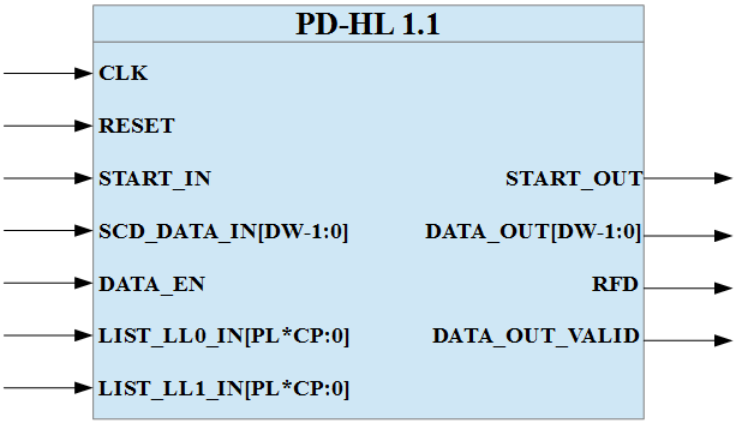

Figure 1: *Block diagram of PD-HL 1.1*

Main programmable parameters of the IP core are listed in Table 1.

Table 1: *PD-HL1.1 Programmable Parameters*

Parameter Name	Symbol	Description
Block Length	BL	Length of a code block. BL has to be a power of 2.
Code Rate	R	Number of data bits divided by BL.
Channel Precision	CP	Number of bits to represent a channel log-likelihood ratio.
Parallelization level	PL	Number of parallel processing units.
Frozen Indices	FI	Frozen indices are read-in from a file.
List Size	LS	Number of decision bits traced concurrently.
Data Width	DW	Width of the data input/output ports.

The I/O ports descriptions are given in Table 2.

Table 2: *I/O Ports of PD-HL 1.1*

Pin	Sense	Port Width	Description
CLK	Input	1	All synchronous logic operations are triggered by rising edge of CLK.
RESET	Input	1	Initializes all variables and signals to their initial state and terminates all operations synchronously.
START_IN	Input	1	Pulses high at the beginning of a new data input block.
DATE_EN	Input	1	Marks valid input data.
LIST_LL0_IN	Input	PL*CP	Log Likelihood LL0 input for list decoder.
LIST_LL1_IN	Input	PL*CP	Log Likelihood LL1 input for list decoder.
SCD_DATA_IN	Input	DW*CP	Log likelihood ratio LLR input.
START_OUT	Output	1	Marks beginning of a data output block.
DATA_OUT	Output	DW	Decision output of decoder.
RFD	Output	1	Indicates decoder is ready to receive a new input data block.
DATA_OUT_VALID	Output	1	Marks valid output data.

Performance

This section details the performance information of the PD-HL 1.1 for various core configurations.

Latency and Interval

Latency is the number of active clock cycles from RFD signal to the DATA_OUT_VALID signal. Interval is the number of active clock cycles between two successive RFD signals

Throughput

Throughput, maximum raw data input rate in Mbps, can be calculated as

$R * BL * (\frac{Fmax(MHz)}{INTERVAL})$.

Behavioral simulation of the PD-SC 1.1 is shown in Figure 2.

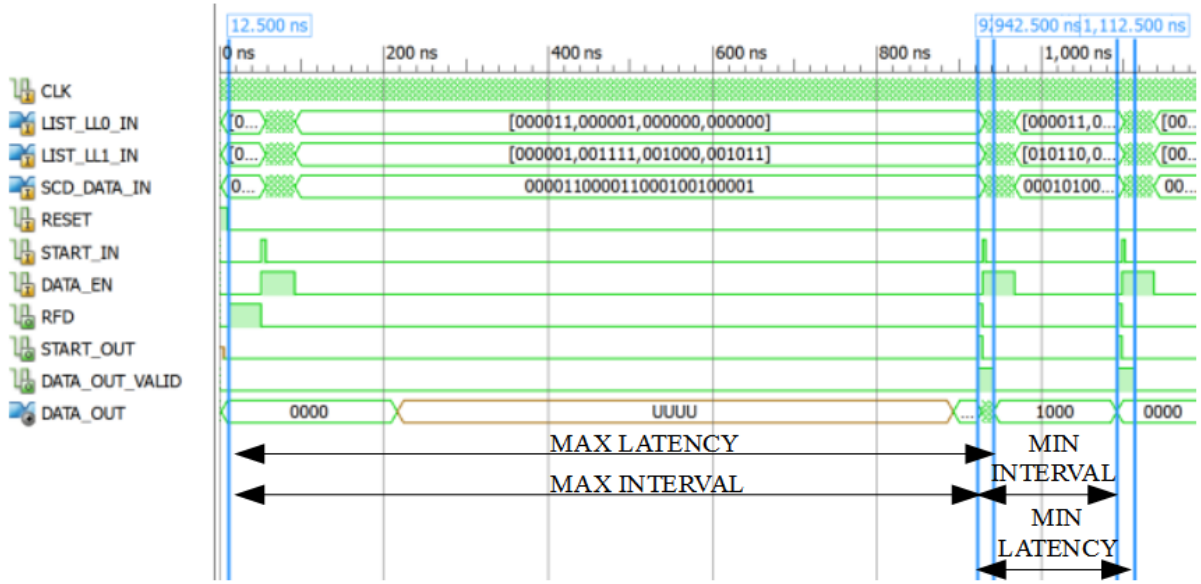

Figure 2: *Xilinx ISIM latency and interval results of PD-HL 1.1 for BL=32, DW=4*

Latency and throughput values are shown in Table 3 for selected configurations.

Table 3: *PD-HL 1.1 Performance Results for Kintex-7, polar codes of rate ½*

Configuration Parameters				**Performance**					
R	**BL**	**DW**	**List Size**	**Min Latency (CC)**	**Min Interval (CC)**	**Max T/P (Mbps)**	**Max Latency (CC)**	**Max Interval (CC)**	**Min T/P (Mbps)**
0.5	256	4	2	187	155	120	1565	1533	12
0.5	256	4	16	187	155	121	1565	1533	12
0.5	1024	4	2	679	551	134	6770	6642	11

Notes:

1) The performance results obtained with Kintex-7 (*XC7K325T-2FFG900C) and* Xilinx FPGA. Throughput may differ for other configurations and FPGAs.

2) Channel and LLR precision are equal to 6.

Resource Utilization

Synthesis and Implementation Results

PD-HL 1.0 synthesized with Xilinx ISE v14.7 and implemented on Xilinx Kintex-7 (XC7K325T-2FFG900C) FPGA KC705 Evaluation Kit. The synthesis and implementation results are shown in Table 4 and Table 5 respectively

Table 4: *PD-HL 1.1 Synthesis Results for Kintex-7*

BL	DW	LS	FFs	LUTs	IOBs	BRAMs	Fmax(MHz)
256	4	2	7773	16278	83	15	146
256	4	16	24251	73990	83	113	146
256	4	32	45054	243745	83	225	147
1024	4	2	27654	57164	83	18	144
1024	4	16	72084	177306	83	130	143

Table 5: *PD-HL 1.1 Implementation Results for Kintex-7(XC7K325T-2FFG900C)*

BL	DW	LS	FFs	LUTs	Slices	FF-LUT Pairs	IOBs	18k BRAMs	36k BRAMs
256	4	2	7813	12588	4798	14402	83	1	14
256	4	16	24291	64804	21326	73331	83	1	112
1024	4	2	27694	44679	12633	46912	83	3	16

Further Information

For further information on product technical specifications, customization to specific applications, sales terms and pricing, please contact info@polaran.com.

PD-HL Revision History

Date	Version	Revision
03/03/15	1.0	First release.
25/11/15	1.1	Updated to version 1.1. Implementation results are added.