Product Brief

Polar Decoder PD-MS 1.1

Main Features

- Implements multi-stage polar successive cancellation decoder
- Supports multi-stage successive cancellation decoding for 16, 64, 256, 1024, 4096 and 16384 QAM
- Implements M-QAM demapper for supported constellation sizes.
- Implements PD-SC successive cancellation decoder with fast architecture.
- Drop-in IP core
- Supports data rates in hundreds of Mb/s on standard FPGAs

General Description

Block diagram of multi-stage polar decoder (PD-MS 1.1) is shown in Figure 1.

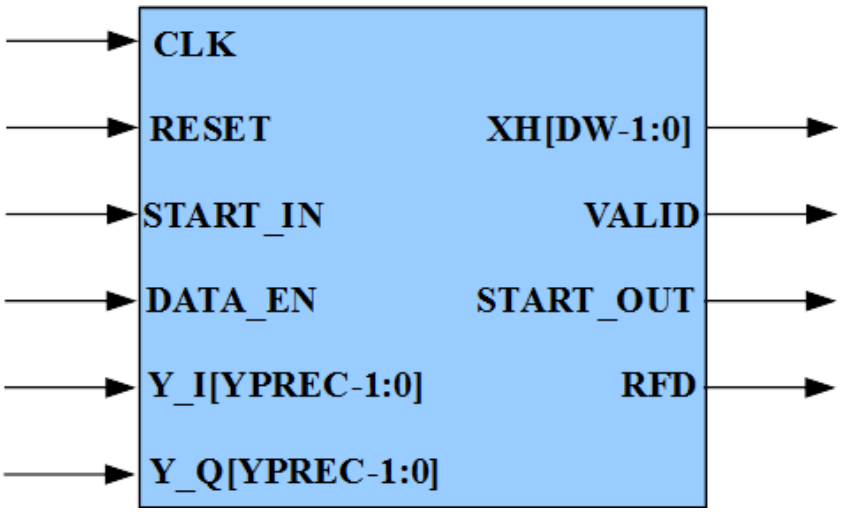


Figure 1: *Block diagram of PD-MS 1.1.*

Top level programmable (generic) parameters of the IP core are listed in Table 1.

Table 1: *PD-MS 1.1 top level programmable parameters.*

Name	Symbol	Description
Block Length	BL	Length of an each code block. BL has to be a power of 2.
Code rate	R	Number of information bits divided by BL.
Channel Precision	YPREC	Number of bits to represent a channel log-likelihood ratio.
Frozen Locations	FIL	Frozen index locations are read-in from a file.
Bit per Symbol	m	Each QAM symbol has m bits. The decoder has m/2 stages.
Data Width	DW	Width of the data input/output ports.

Internal generic parameters of the IP core are listed in Table 2.

Table 2: *PD-MS 1.1 internal programmable parameters.*

Name	Symbol	Description
Total Block Length	TBL	Length of the total code block, BL*m/2.
Constellation Size	M	M-QAM demodulation for each decoder stage, 2^m.
LLR Precision	LLRPREC	Fast-SCD input and de-mapper output data precision.

The I/O ports descriptions are given in Table 3.

Table 3: *I/O Ports of PD-MS 1.1.*

Pin	Sense	Port Width (bits)	Description
CLK	Input	1	*Clock.* All synchronous logic operations are triggered by rising edge of CLK.
RESET	Input	1	*Synchronous Reset.* Initializes the decoder to initial state synchronously.
START_IN	Input	1	*Start Input.* Marks the beginning of a new input block.
DATA_EN	Input	1	*Data Enable.* Marks valid input data.
Y_I	Input	YPREC	*Channel In-phase Component.* Decoder input-1
Y_Q	Input	YPREC	*Channel Quadrature Component.* Decoder input-2
XH	Output	DW	*Decision Estimation.* Decoder output (consists of information bits and frozen bits).
START_OUT	Output	1	*Start Output.* Marks the beginning of a new data output block.
VALID	Output	1	*Valid Output Data.* Marks valid output data.
RFD	Output	1	*Ready for Data*. Indicates decoder is ready to receive a new input data block.

Performance

This section contains the performance results of PD-MS 1.1 for various core configurations.

Latency is defined as the number of rising clock edges from START_IN pulse to the last active pulse of VALID.

Interval is defined as the number of rising clock edges between the first rising edge point of RFD to the next falling edge point of RFD. That means the number of active RFD cycles are reported as interval.

Throughput, maximum raw data input rate in Mbps, can be calculated as

$$R * N * (\frac{Fmax(MHz)}{Interval}).$$

Latency, interval and throughput values are shown in Table 4 for particular decoder configurations.

Table 4: *PD-MS 1.1 performance results for Xilinx Kintex-7 (XC7K325T-2FFG900C) FPGA KC705 Evaluation Kit, R = 0.5, DW = 4, YPREC = 20, LLRPREC = 8.*

Generic Parameters		Performance		
M	**TBL**	**Latency (CC)**	**Interval (CC)**	**Throughput (Mbps)**
16	128	157	59	162
	512	457	200	153
64	192	174	112	100
	768	613	376	117
256	256	242	180	87
	1024	749	543	108
1024	320	262	200	92
	1280	883	667	110
4096	384	330	268	84
	1536	1038	832	106
16384	448	350	288	88
	1792	1166	951	108

Resource Utilization

Synthesis and Implementation Results

PD-MS 1.1 synthesized with Xilinx ISE v14.7 and implemented on Xilinx Kintex-7 (XC7K325T-2FFG900C) FPGA KC705 Evaluation Kit. The synthesis and implementation results are shown in Table 5 and Table 6 respectively.

Table 5: *PD-MS 1.1 synthesis results for Xilinx Kintex-7 (XC7K325T-2FFG900C) FPGA KC705 Evaluation Kit, R = 0.5, DW = 4, YPREC = 20, LLRPREC = 8.*

Generic Parameters		Synthesis Results				
M	**TBL**	**FFs**	**LUTs**	**IOBs**	**BRAM-36**	**Fmax(MHz)**
16	128	3840	7412	71	0	149
	512	14260	28583	71	3	119
64	192	5596	10621	71	0	117
	768	21597	42630	71	4	115
256	256	7316	12915	71	0	123
	1024	27881	51639	71	5	114

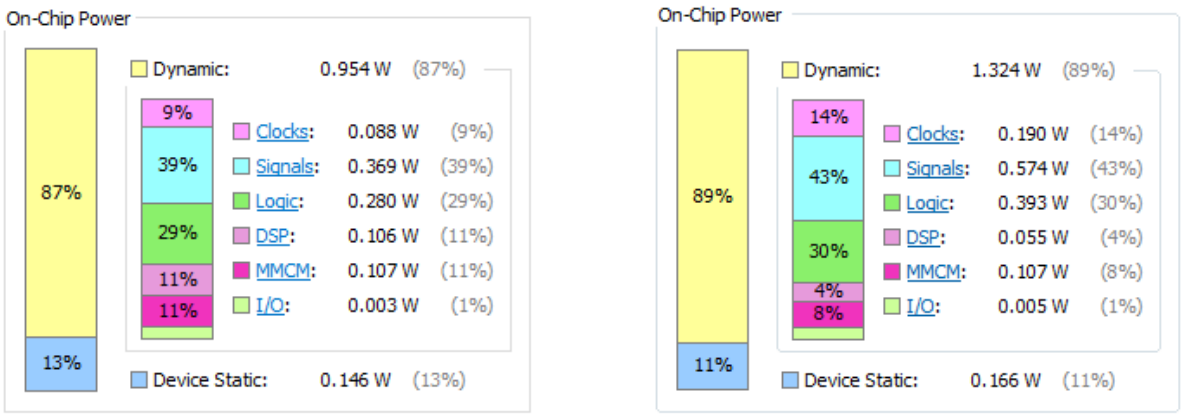
1024	320	9017	15789	71	0	115
	1280	34154	61018	71	6	115
4096	384	10743	18412	71	0	118
	1536	40367	71156	71	7	114
16384	448	12459	21853	71	0	113
	1792	48847	92116	71	8	114

Table 6: *PD-MS 1.1 implementation results for Xilinx Kintex-7 (XC7K325T-2FFG900C) FPGA KC705 Evaluation Kit, R = 0.5, DW = 4, YPREC = 20, LLRPREC = 8.*

Generic Parameters		**Implementation Results**				
M	**TBL**	**FFs**	**LUTs**	**IOBs**	**BRAM-36**	**Fmax(MHz)**
16	128	3876	6873	71	0	137
	512	14364	27012	71	2.5	127
64	192	5684	9610	71	0	127
	768	21701	39142	71	3.5	120
256	256	7352	11797	71	0	115
	1024	28021	47212	71	4.5	112
1024	320	9017	14341	71	0	113
	1280	34259	55914	71	5.5	108
4096	384	10784	16792	71	0	110
	1536	40492	65966	71	6.5	107
16384	448	12550	19799	71	0	110
	1792	48951	86122	71	7.5	101

Power Consumption

Power consumption of PD-MS is shown for 256 and 16384 QAM in Figure 2. The first implementation has 1024 block length and 512 information bits, implemented on Artix FPGA. The implementation has total 1.1 W power usage consist of 0.146 W static and 0.954 dynamic. Routing signals and complex logic operations cause 39% and 29% of the dynamic power usage, because semi-parallel implementation is used. In addition to that, the second implementation has implemented on Kintex FPGA. The implementation has total 1.49 W power usage consists of 0.166 W static and 1.324 W dynamic. Similar to 256-QAM implementation, the implementation complexity mainly caused by routing signals and logic operations. In those implementations, the throughput of decoder is 183 Mb/s for 256-QAM and 142 Mb/s for 16384-QAM. Therefore, the power consumption is 8.8 nJ/bit for 256-QAM and 12.86 nJ/bit for 16384-QAM.

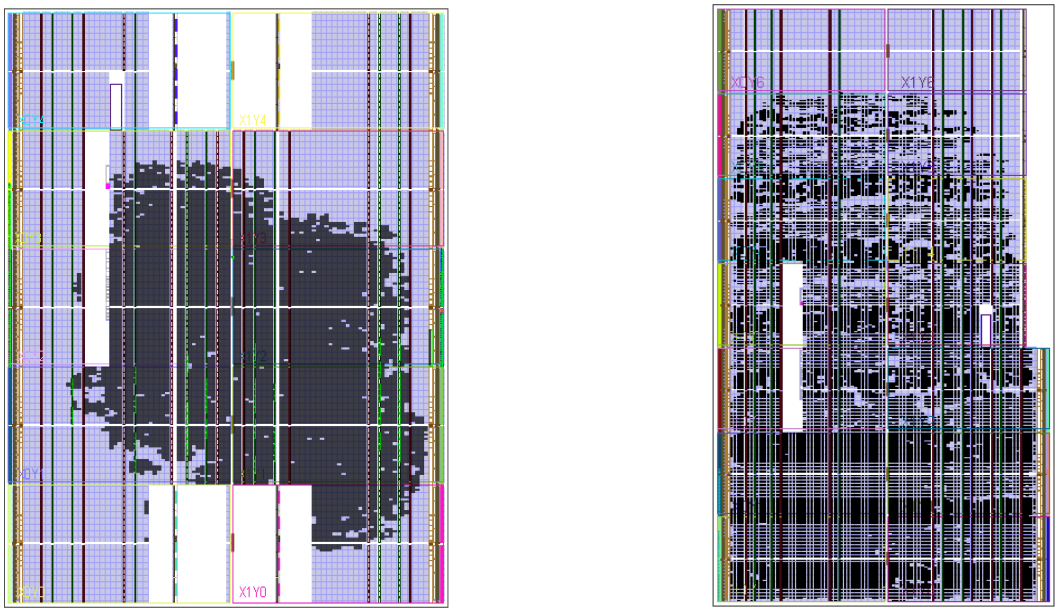


a) (1024,512) 256-QAM on Artix. *b) (1792,896) 16384-QAM on Kintex.*

Figure 2: *Power consumption of PD-MS 1.1 (1024,512) 256-QAM and (1792,896) 16384-QAM on Xilinx Artix and Kintex FPGA.*

Implementation Overview on FPGA

Implementation overview of 256-QAM with 1024 block length and 16384-QAM with 1792 are shown in Figure 3. 16384-QAM implementation has significantly higher area than 256-QAM implementation due to logic complexity.



a) (1024,512) 256-QAM on Artix. *b) (1792,896) 16384-QAM on Kintex.*

Figure 3: *Implementation overview of PD-MS 1.1 (1024,512) 256-QAM and (1792,896) 16384-QAM on Artix and Kintex FPGA.*

Further Information

For further information on product technical specifications, customization to specific applications, sales terms and pricing, please contact info@polaran.com.

PD-MS Revision History

Date	Version	Revision
30/11/2015	1.0	Initial release.
04/08/2016	1.1	Spelling mistakes are corrected. Power consumption is added. Implementation overview is added.