Product Brief

Polar Decoder PD-SC 1.1

Main Features

- Implements the successive cancellation decoding algorithm for polar codes
- Drop-in IP core
- Supports data rates in hundreds of Mb/s on standard FPGAs

General Description

Block diagram of PD-SC 1.1 is shown in Figure 1.

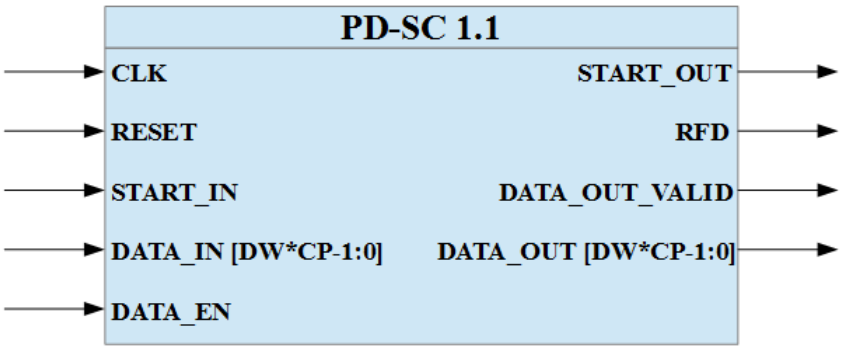

Figure 1: *Block diagram of PD-SC 1.1*

Main programmable parameters of the IP core are listed in Table 1.

Table 1: PD-SC 1.1 Programmable Parameters

Parameter Name	Symbol	Description
Block Length	BL	Length of a code block. BL has to be a power of 2.
Code rate	R	Number of data bits divided by BL.
Channel Precision	CP	Number of bits to represent a channel log-likelihood ratio.
Frozen Indices	FI	Frozen indices are read-in from a file.
Data Width	DW	Width of the data input/output ports.

The I/O ports descriptions are given in Table 2.

Table 2: *I/O Ports of PD-SC 1.1*

Pin	Sense	Port Width (bits)	Description
CLK	Input	1	*Clock.* All synchronous logic operations are triggered by rising edge of CLK.
RESET	Input	1	*Synchronous Reset.* Initializes the decoder to initial state synchronously.
DATA_IN	Input	DW*CP	*Input Data.* Channel log-likelihood-ratio values.
DATA_EN	Input	1	*Data Enable.* Marks valid input data.
START_IN	Input	1	*Start Input.* Marks the beginning of a new data input block.
DATA_OUT	Output	DW	*Output Data.* Decoder output (consists of information bits and frozen bits).
START_OUT	Output	1	*Start Output.* Marks the beginning of a new data output block.
RFD	Output	1	*Ready for Data*. Indicates decoder is ready to receive a new input data block.
DATA_OUT_VALID	Output	1	*Valid Output Data.* Marks valid output data.

Performance

This section details the performance information of the PD-SC 1.1 for various core configurations.

Latency and Interval

Latency is the number of active clock cycles from RFD signal to the DATA_OUT_VALID signal. Interval is the number of active clock cycles between two successive RFD signals

Throughput

Throughput, maximum raw data input rate in Mbps, can be calculated as

$$R * BL * (\frac{Fmax(MHz)}{INTERVAL}).$$

Behavioral simulation of the PD-SC 1.1 is shown in Figure 2.

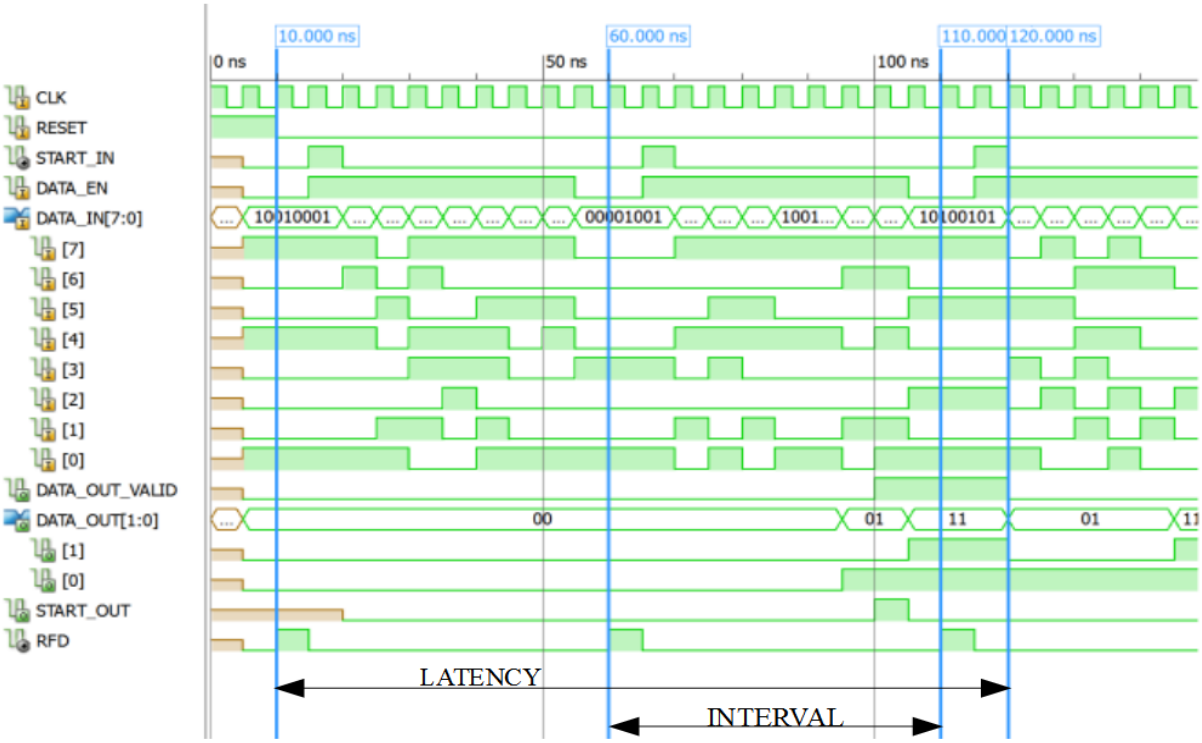

Figure 2: *Xilinx ISIM latency and interval results of PD-SC 1.1 for BL=16, DW=2*

Latency, interval and throughput values are shown in Table 3 and Table 4 for selected configurations.

Table 3: *PD-SC 1.1 Performance Results for Kintex-7, polar codes of rate ½*

Configuration Parameters		Performance		
BL	**DW**	**Latency (CC)**	**Interval (CC)**	**Throughput (Mbps)**
128	4	118	69	209
256	4	184	87	258
512	4	358	165	261
1024	4	676	291	304

Table 4: *PD-SC 1.1 Performance Results for Artix-7, polar codes of rate ½*

Configuration Parameters		Performance		
BL	**DW**	**Latency (CC)**	**Interval (CC)**	**Throughput (Mbps)**
128	4	118	69	151
256	4	184	87	199
512	4	358	165	203
1024	4	676	291	224

Notes:

1) The performance results obtained with Kintex-7 (*XC7K325T-2FFG900C) and* Artix-7 *(XC7A200T-2FBG676C*) Xilinx FPGAs. Throughput may differ for other configurations and FPGAs.
2) Channel and LLR precision are equal to 4.

Resource Utilization

Synthesis and Implementation Results

PD-SC 1.1 has been synthesized with Xilinx ISE v14.7. The synthesis results for resource usage and maximum clock frequency are shown in Table 5 and Table 6. PD-SC 1.1 has been implemented on Kintex-7(*XC7K325T-2FFG900C)* and Artix-7 *(XC7A200T-2FBG676C*) Xilinx FPGAs. The implementation results for resource usage are shown in Table 7 and Table 8.

Table 5: *PD-SC 1.1 Synthesis Results for Kintex-7*

BL	DW	FFs	LUTs	IOBs	BRAMs	BUFGs	Fmax(MHz)
128	4	1891	4238	26	1	1	225
256	4	3733	8284	26	1	1	176
512	4	7327	16374	26	1	1	168
1024	4	14502	33206	26	2	1	173

Table 6: *PD-SC 1.1 Synthesis Results for Artix-7*

BL	DW	FFs	LUTs	IOBs	BRAMs	BUFGs	Fmax(MHz)
128	4	1889	4206	26	1	1	163
256	4	3733	8279	26	1	1	135
512	4	7328	17097	26	1	1	131
1024	4	14503	33102	26	2	1	127

Table 7: *PD-SC 1.1 Implementation Results for Kintex-7(XC7K325T-2FFG900C)*

BL	DW	FFs	LUTs	Slices	FF-LUT Pairs	IOBs	18k BRAMs	36k BRAMs
128	4	1891	3402	1331	3870	26	1	0
256	4	3733	6646	2515	7783	26	1	0
512	4	7327	12473	4797	15076	26	2	0
1024	4	14502	26978	9390	30089	26	1	1

Table 8: *PD-SC 1.1 Implementation Results for Artix-7 (XC7A200T-2FBG676C)*

BL	DW	FFs	LUTs	Slices	FF-LUT Pairs	IOBs	18k BRAMs	36k BRAMs
128	4	1889	3323	1666	3973	26	1	0
256	4	3733	6654	2415	7605	26	1	0
512	4	7328	13412	3878	14375	26	2	0
1024	4	14503	26889	10035	30110	26	1	1

Further Information

For further information on product technical specifications, customization to specific applications, sales terms and pricing, please contact info@polaran.com.

PD-SC Revision History

Date	Version	Revision
03/03/15	1.0	Initial release.
25/03/15	1.1	Updated to version 1.1. Implementation results are added.