Polar Combinational Encoder (PE-CB-100G) v1.1

Features

- Supports 7-Series Xilinx FPGAs (Artix-7, Kintex-7, Virtex-7)
- Implements Polar Combinational Encoder for 3rd generation FEC, 100 Gb/s optical networks and beyond
- Satisfies Cloud radio access network (C-RAN) fronthaul requirements in terms of high data throughput, low latency and low energy consumption
- Compatible with both Polar and Reed-Muller (RM) codes
- Compatible with the decoder IP core products of POLARAN: Polar Successive Cancellation (SC) Decoder, Polar-SC-List Decoder, Polar-SC-Hybrid Decoder, Majority-Logic Decoder
- Implements "Fully Combinational" encoding architecture
- Adjustable I/O port size with respect to code block length (N), code rate (R) and payload (K)
- Supports N ∈{256, 512, 1024} and R ∈ {3/4, 4/5, 15/16}
- Supports 100 Gb/s data speed, 2 clock cycles latency and 1 cycle interval for each consecutive payload
- Compatible with Xilinx Vivado versions greater than 2016.1

General Description

The Polar Combinational Encoder is designed for C-RAN fronthaul to transmit In-phase and Quadrature components of the signal from Remote Radio Heads (RRH) to Baseband Unit (BBU) Pool through optical links. The combinational encoder satisfies the low latency and high throughput requirements of the optical link between RRH and BBU. The encoder can exceed 100 Gb/s for the code block length N greater than 512.

The encoder is compatible with the IP core products of POLARAN: Polar-SC Decoders and Majority-Logic Decoder.

For the use of this IP Core, there are three options for the block length (N) which are 1024, 512, 256. There are three rate options which are 15/16, 4/5, 3/4.

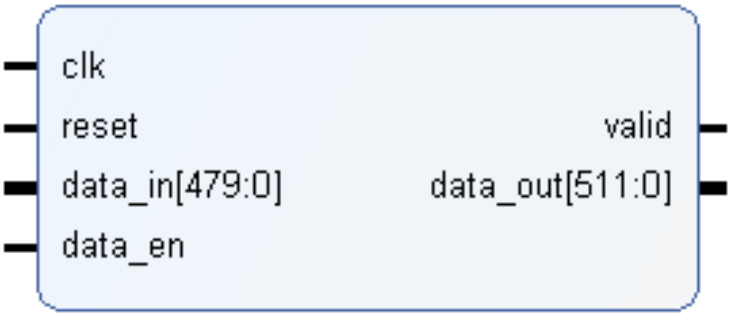

Figure 1: IP Core of Combinational Encoder (N=512, R=15/16)

Input/Output Ports

The descriptions of I/O ports of the Polar Combinational Encoder are stated in Table 2.

Table 2: I/O Ports

Pin	Sense	Port Width (bits)	Description
CLK	Input	1	***Clock.*** All synchronous logic operations are triggered by rising edge of CLK.
RESET	Input	1	***Synchronous Reset.*** Initializes all variables and signals to their initial state and terminates all operations synchronously.
DATA_IN	Input	K	***Input Data.*** The payload is given to the encoder through this port. The port width of the payload is K.
DATA_EN	Input	1	***Data Enable.*** Marks the valid input data.
DATA_OUT	Output	N	***Output Data.*** Consists of information bits and parity bits.
VALID	Output	1	***Valid Output Data.*** Marks the valid output data.

Further explanations about I/O ports are shown below.

Clock (CLK)

All synchronous logic operations of the system are triggered by rising edge of the Clock (CLK).

Synchronous Reset (RESET)

If RESET pin is high, all variables and signals are reset to their initial states and all logic operations are terminated synchronously.

Data Enable (DATA_EN)

Input data must be applied when data enable is high, otherwise it is discarded.

Input Data (DATA_IN)

Encoder accepts data from this pin. Input data consists of information bits. At each clock cycle, data width of input data can be applied to the encoder. The data width of that port is equal to the payload length, “K”.

Output Data (DATA_OUT)

The encoded data is written on the **data_out** port in fully-parallel manner. The data width of that port is called “N”. The output data consists of both information and parity bits.

Functional Description of Polar Combinational Encoder

The behavioral simulation of Polar Combinational Encoder is shown in Figure 2.

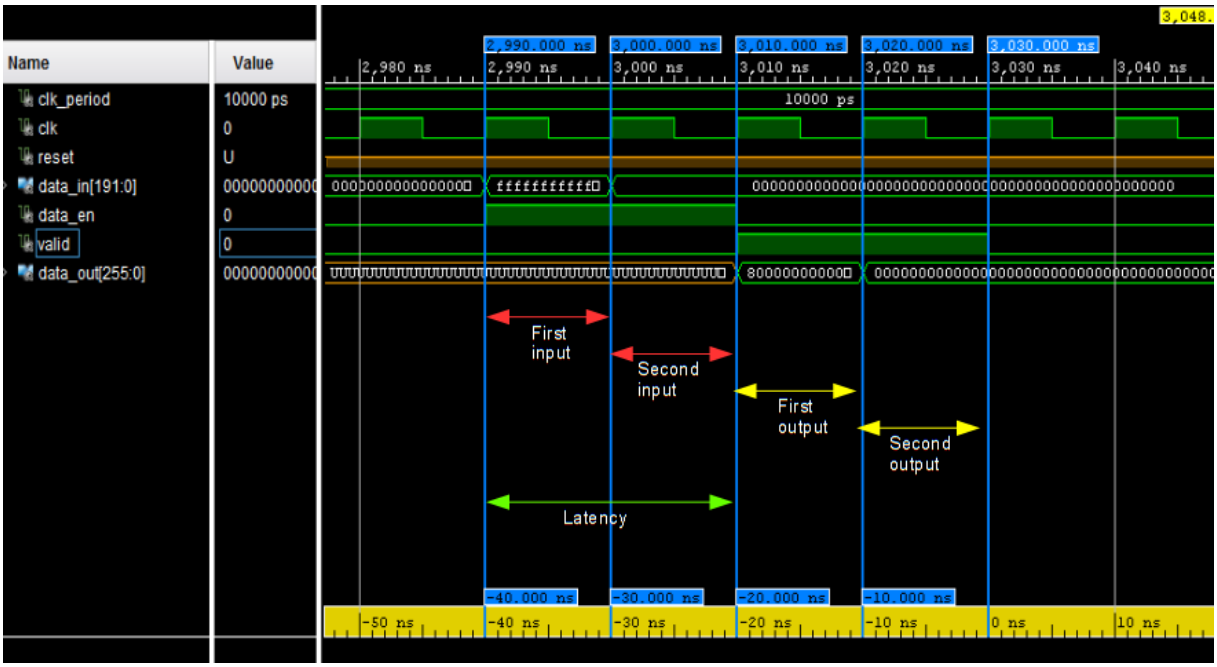

Figure 2: The Behavioral Simulation of Polar Combinational Encoder (N=256, R=3/4)

Latency of encoder is time interval between rising edge of **data_en** signal and **valid** signal. Combinational encoder has constant 2 clock cycle latency. The latency of this encoder doesn't vary when block length and code rate change. Input data is read from **data_in** port of encoder when **data_en** is high. After encoding operation is completed, **valid** marks the valid output data of encoder. Valid output data can be read from **data_out** port. The encoder is ready for new input data at each clock cycle due to the pipeline implementation.

Detailed Information of Polar Combinational Encoder

Polar combinational encoder is implemented on Kintex-7 Xilinx FPGA. Vivado performance results for maximum clock frequency, latency and throughput are shown in Table 3.

Table 3: Polar Combinational Encoder Performance Results

FPGA Type	Block Length (N)	Coding Rate (R)	Resource Usage				Clock Freq. (MHz)	Throughput (Gb/s)
			LUT		FF			
			Num.	%	Num.	%		
Kintex-7 (xc7k325)	256	3/4	602	0.295	451	0.11	200	38.4
		4/5	593	0.290	463	0.113	200	30.75
		15/16	629	0.3	500	0.122	200	48
	512	3/4	1378	0.676	900	0.22	200	76.8
		4/5	1380	0.677	925	0.226	200	82
		15/16	1431	0.702	995	0.244	200	96
	1024	3/4	5060	2.48	1796	0.44	150	115.2
		4/5	5135	2.51	1848	0.453	150	123
		15/16	5612	2.75	1987	0.487	100	96

Document Changelog

Version	Publish Date	Changed Content/Page	Reason
1.0	23.10.2017	Whole report	First version of the report was written.
2.0	18.01.2018	Whole report	Product name was updated.