Product Brief

Polar Encoder PE-MS 1.1

Main Features

- Implements multi-stage encoding algorithm for polar codes
- Supports multi-stage encoding for 16, 64, 256, 1024, 4096 and 16384 QAM
- Implements M-QAM mapper for supported constellation sizes
- Drop-in IP core
- Supports data rates in hundreds of Mb/s on standard FPGAs
- Implements $\log_2(M)/2$ polar code construction for each level of QAM such that in-phase and quadrature components coded together

General Description

Block diagram of PE-MS 1.1 is shown in Figure 1.

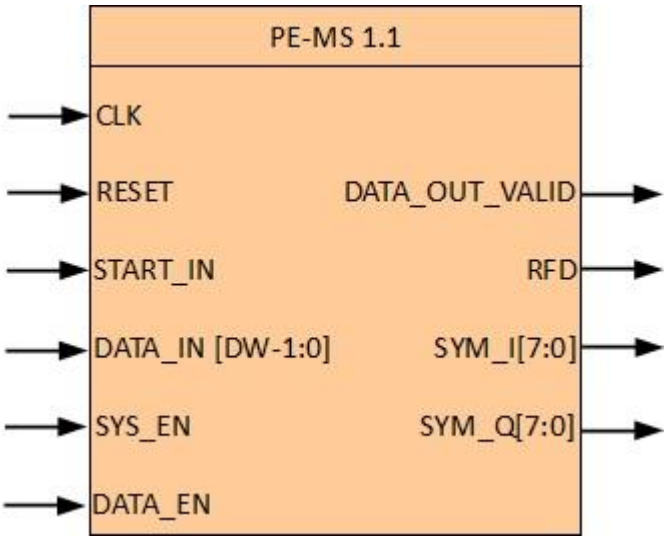


Figure 1: *Block diagram of PE-MS 1.1.*

Main programmable parameters of the IP core are listed in Table 1.

Table 1: *PE-MS 1.1Top Level programmable parameters.*

Name	Symbol	Description
Block Length	BL	Length of an each code block. BL has to be a power of 2.
Code rate	R	Number of information bits divided by BL.
Frozen Locations	FIL	Frozen index locations are read-in from a file.
Bit per Symbol	m	Each QAM symbol has m bits. The encoder has m/2 stages.
Data Width	DW	Width of the data input/output ports.

Internal generic parameters of the IP core are listed in Table 2.

Table 2: *PE-MS 1.1 internal programmable parameters.*

Name	Symbol	Description
Total Block Length	TBL	Length of the total code block, BL*m/2.
Constellation Size	M	M-QAM modulation for each encoder stage, 2^m.

The I/O ports descriptions are given in Table 3.

Table 3: *I/O Ports of PE-MS 1.1*

Pin	Sense	Port Width (bits)	Description
CLK	Input	1	*Clock.* All synchronous logic operations are triggered by rising edge of CLK.
RESET	Input	1	*Synchronous Reset.* Initializes all variables and signals to their initial state synchronously.
SYS_EN	Input	1	*Systematic Enable*. Selects standard or systematic encoding operation.
START_IN	Input	1	*Start Input.* Marks the beginning of a new data input block.
DATA_EN	Input	1	*Data Enable.* Marks valid input data.
DATA_IN	Input	DW	*Data input*. Contains frozen and information data.
SYM_I	Output	8	*Channel In-phase Component.* Encoder output-1
SYM_Q	Output	8	*Channel Quadrature Component.* Encoder output-2
DATA_OUT_VALID	Output	1	*Valid Output Data.* Marks valid output data.
RFD	Output	1	*Ready for Data.* Indicates the encoder is ready for new data input.

Performance

This section contains the performance results of PE-MS 1.1 for various core configurations.

Latency is defined as the number of rising clock edges from START_IN pulse to the following pulse of DATA_OUT_VALID.

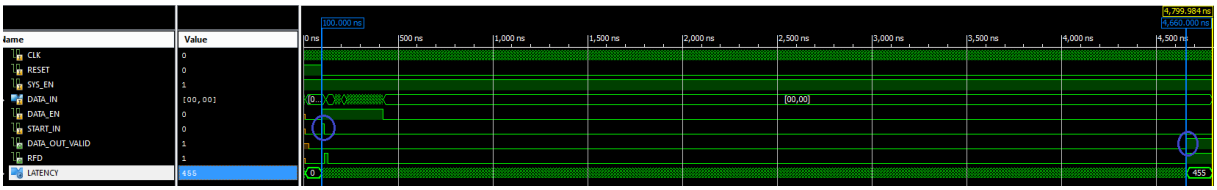


Figure 2: *Xilinx ISIM latency results for TBL = 128.*

Throughput, maximum raw data input rate in Mbps, can be calculated as

$$R * TBL * (\frac{Fmax(MHz)}{Interval}).$$

Latency and throughput values are shown in Table 4 for particular encoder configurations.

Table 4: *PE-MS 1.1 performance results for Xilinx Kintex-7 (XC7K325T-2FFG900C) FPGA KC705 evaluation kit, R = 1, DW = 2.*

Generic Parameters		Performance	
M	**TBL**	**Latency(CC)**	**Throughput (Mbps)**
16	128	455	98
	512	2311	77
64	192	455	147
	768	2311	116
256	256	455	196
	1024	2311	155
1024	320	455	246
	1280	2311	193
4096	384	455	295
	1536	2311	232
16384	448	455	344
	1792	2311	271

Resource Utilization

Synthesis and Implementation of IP Core

PE-MS 1.1 synthesized with Xilinx ISE v14.7 and Vivado 2016.1 and implemented on Xilinx Kintex-7 (XC7K325T-2FFG900C) FPGA KC705 Evaluation Kit. The synthesis and implementation results are shown in Table 5 and Table 6 respectively.

Table 5: *PE-MS 1.1 synthesis results for Xilinx Kintex-7 (XC7K325T-2FFG900C) FPGA KC705 evaluation kit, R = 1, DW = 2.*

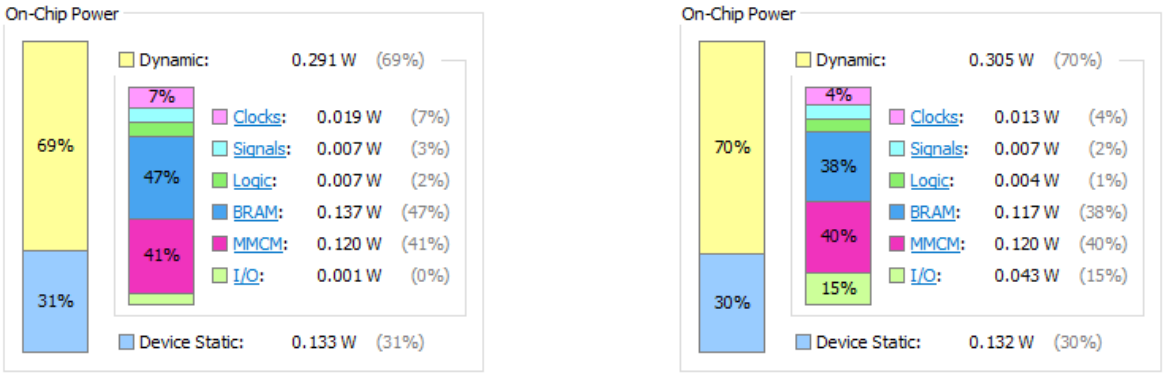
Generic Parameters		Synthesis Results				
M	**TBL**	**FFs**	**LUTs**	**IOBs**	**BRAMs**	**Fmax (MHz)**
16	128	67	104	27	17	349
	512	91	185	27	17	349
64	192	79	121	29	18	349
	768	97	210	29	18	349
256	256	85	133	31	18	349
	1024	103	234	31	18	349
1024	320	89	137	33	19	349
	1280	106	252	33	19	349
4096	384	95	148	35	19	349
	1536	113	278	35	19	349
16384	448	99	148	37	20	349
	1792	118	298	37	20	349

Table 6: *PE-MS 1.1 implementation results for Xilinx Kintex-7 (XC7K325T-2FFG900C) FPGA KC705 evaluation kit, R = 1, DW = 2.*

Generic Parameters		Implementation Results						
M	**TBL**	**FFs**	**LUTs**	**Slices**	**IOBs**	**18k BRAMs**	**36k BRAMs**	**Fmax(MHz)**
16	128	75	89	54	27	2	16	317
	512	91	148	78	27	2	16	308
64	192	79	94	53	29	3	16	313
	768	97	174	186	29	3	16	292
256	256	85	104	73	31	4	16	324
	1024	103	193	92	31	4	16	308
1024	320	89	109	69	33	5	16	300
	1280	106	210	118	33	5	16	306
4096	384	95	116	79	35	6	16	276
	1536	113	236	139	35	6	16	278
16384	448	99	124	88	37	7	16	291
	1792	118	265	141	37	7	16	299

Power Consumption

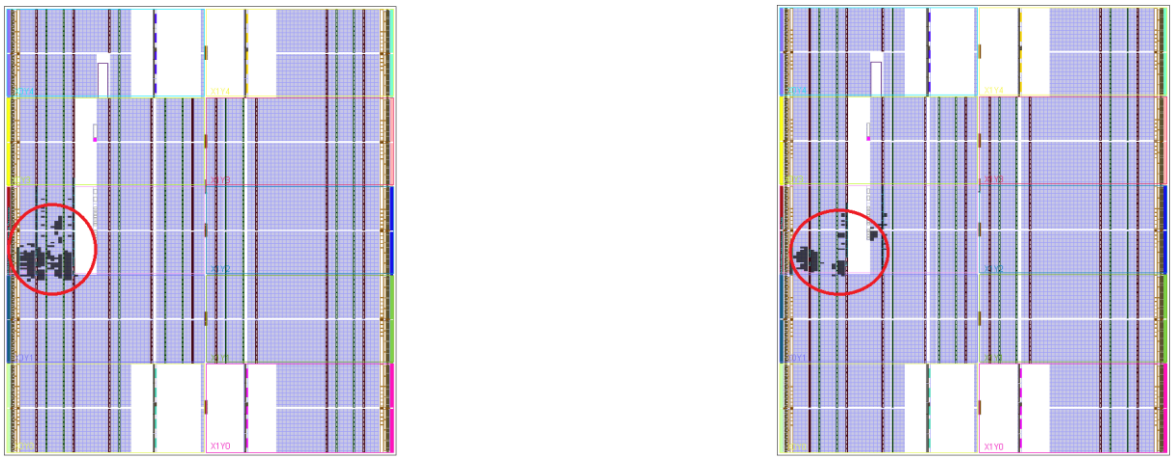
Power consumption of PE-MS 1.1 on Xilinx Artix FPGA is shown in Figure 3. For 16384-QAM, PE-MS IP core has total 0.424 W power consumption, which consists of 0.133 W static and 0.291 W dynamic power consumption. PE-MS uses much more memory than the logic such that 47% of dynamic power usage caused by BRAM and only 2% power usage caused by logic. The power usage of 256-QAM and 1634-QAM results is almost the same such that the complexity of encoder scales well with the constellation size. In addition to that, 256-QAM implementation has 129 Mb/s; 16384-QAM implementation has 219 Mb/s throughput. Therefore, the power consumption is calculated as 1,28 nJ/bit for 256-QAM and 1,42 nJ/bit when the I/O power usage is excluded.



a) 16384-QAM *b) 256-QAM*

Figure 3: *256-QAM (1024, 512) and 16384-QAM (1792,869) PE-MS power consumption on Xilinx Artix FPGA.*

Implementation Overview on FPGA



a) 16384-QAM *b) 256-QAM*

Figure 4: *256-QAM (1024, 512) and 16384-QAM (1792,869) PE-MS implementation overview on Xilinx Artix FPGA.*

The implementation overview of PE-MS is shown in Figure 4. 16384-QAM implementation

uses more resources and area than the 256-QAM implementation since the block size and the constellation size increases from 1024 to 1792 and 256 to 16384 respectively.

Further Information

For further information on product technical specifications, customization to specific applications, sales terms and pricing, please contact info@polaran.com.

PE-NE Revision History

Date	Version	Revision
30/11/2015	1.0	Initial release.
04/08/2016	1.1	Spelling mistakes are corrected. Power consumption is added. Implementation overview is added.