Product Brief

Polar Encoder PE-NE 1.1

Main Features

- Implements the standard (non-systematic) encoding algorithm for polar codes
- Drop-in IP core
- Supports data rates in hundreds of Mb/s on standard FPGAs

General Description

Block diagram of PE-NE 1.1 is shown in Figure 1.

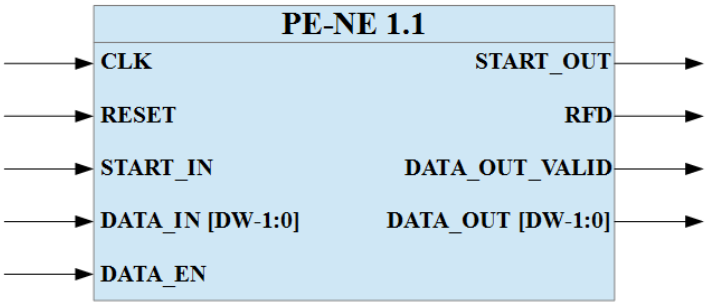

Figure 1: *Block diagram of PE-NE 1.1*

Main programmable parameters of the IP core are listed in Table 1.

Table 1: *PE-NE 1.1 programmable parameters*

Parameter Name	Symbol	Description
Block Length	BL	Length of a code block. BL has to be a power of 2.
Code Rate	R	Number of data bits divided by BL.
Frozen Indices	FI	Frozen indices are read-in from a file.
Data Width	DW	Width of the data input/output ports.

The I/O ports descriptions are given in Table 2.

Table 2: *I/O ports of PE-NE 1.1*

Pin	Sense	Port Width (bits)	Description
CLK	Input	1	All synchronous logic operations are triggered by rising edge of CLK.
RESET	Input	1	Initializes all variables and signals to their initial state synchronously.
DATA_IN	Input	DW	Data input (frozen and information).
START_IN	Input	1	Marks the beginning of a new data input block.
DATA_EN	Input	1	Marks valid input data.
DATA_OUT	Output	DW	Data output (codeword).
START_OUT	Output	1	Marks the beginning of a new data output block.
DATA_OUT_VALID	Output	1	Marks valid output data.
RFD	Output	1	Indicates the encoder is ready for new data input.

Performance

This section details the performance information of the PE-NE 1.1 for various core configurations.

Latency and Interval

Latency is the number of active clock cycles from RFD signal to the DATA_OUT_VALID signal. Interval is the number of active clock cycles between two successive RFD signals

Throughput

Throughput, maximum raw data input rate in Mbps, can be calculated as

$$R * BL * (\frac{Fmax(MHz)}{INTERVAL}).$$

Behavioral simulation of the PE-NE 1.1 is shown in Figure 2.

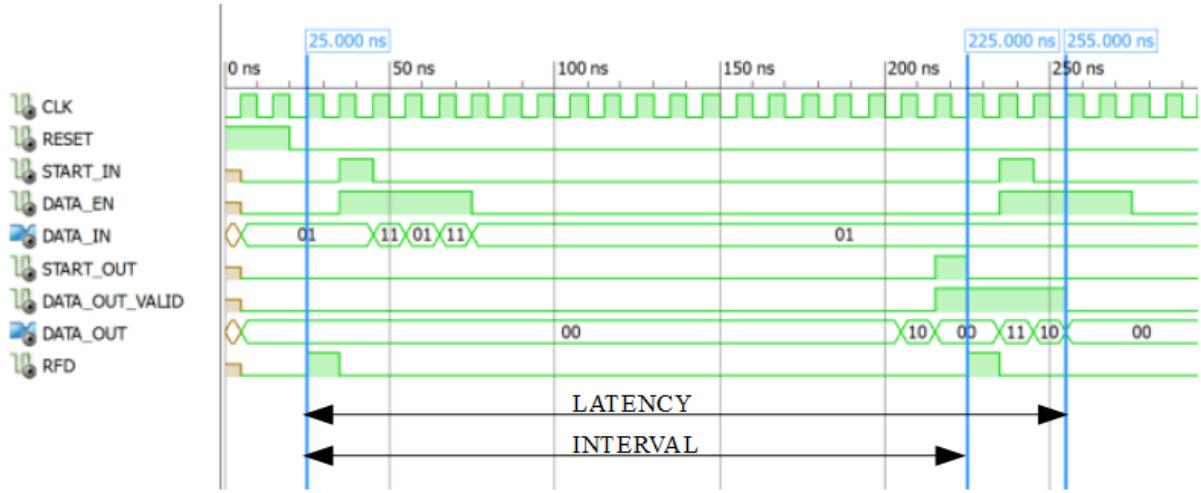

Figure 2: *Xilinx ISIM latency and interval results of PE-NE 1.1 for BL=8, DW =2.*

Latency, interval and throughput values are shown in Table 3 for selected configurations.

Table 3: *PE-NE 1.1 performance results for Xilinx Kintex-7 (XC7K325T-2FFG900C) FPGA KC705 Evaluation Kit, R = 1*

BL	DW	Latency (CC)	Interval (CC)	Throughput (Mbps)
128	4	259	228	189
	8	115	100	378
	16	51	44	844
1024	4	2819	2564	134
	8	1283	1156	262
	16	579	516	576
16384	4	61443	57348	89
	8	28675	26628	182
	16	13315	12292	387

Following table provides formulas in order to calculate latency, interval and throughput if other configurations are preferred.

Table 4: *PE-NE 1.0 latency, interval and throughput Formulas*

Performance	Standard Encoding
Latency (CC)	$3 * \left(\frac{BL}{DW}\right) + \left(\frac{BL}{DW}\right) * \log_2\left(\frac{BL}{DW}\right) + 3$
Interval (CC)	$2 * \left(\frac{BL}{DW}\right) + \left(\frac{BL}{DW}\right) * \log_2\left(\frac{BL}{DW}\right) + 4$
Throughput (Mbps)	$R * BL * (\frac{Fmax(MHz)}{INTERVAL})$.

Resource Utilization

Synthesis and Implementation of IP Core

PE-NE 1.1 synthesized with Xilinx ISE v14.7 and implemented on Xilinx Kintex-7 (XC7K325T-2FFG900C) FPGA KC705 Evaluation Kit. The synthesis and implementation results are shown in Table 4 and Table 5 respectively.

Table 4: *PE-NE 1.1 synthesis results for Xilinx Kintex-7 (XC7K325T-2FFG900C) FPGA KC705 Evaluation Kit, R = 0.5*

BL	DW	FFs	LUTs	IOBs	BRAMs	Fmax (MHz)
128	4	52	99	14	1	336
	8	51	99	22	1	296
	16	54	120	38	1	290
1024	4	74	154	14	1	336
	8	73	152	22	1	296
	16	76	141	38	1	290
16384	4	102	220	14	1	312
	8	101	201	22	1	296
	16	104	215	38	1	290

Table 5: *PE-NE 1.1 implementation results for Xilinx Kintex-7 (XC7K325T-2FFG900C) FPGA KC705 Evaluation Kit, R = 0.5*

BL	DW	FFs	LUTs	Slices	IOBs	18k BRAMs	36k BRAMs	DSP48s	BUFGs
128	4	52	75	44	14	1	0	0	1
	8	51	78	34	22	1	0	0	1
	16	54	99	47	38	1	0	0	1
1024	4	74	131	54	14	1	0	0	1
	8	73	124	53	22	1	0	0	1
	16	76	141	65	38	1	0	0	1
16384	4	102	185	66	14	1	0	0	1
	8	101	167	57	22	1	0	0	1
	16	104	189	73	38	1	0	0	1

Further Information

For further information on product technical specifications, customization to specific applications, sales terms and pricing, please contact info@polaran.com.

PE-NE Revision History

Date	Version	Revision
03/03/15	1.0	Initial release.
25/11/15	1.1	Updated to version 1.1. Implementation results are added.