Product Brief

Polar Encoder PE-SE 2.1

Main Features

- Implements the standard or the systematic encoding algorithm for polar codes
- Drop-in IP core
- Supports data rates in hundreds of Mb/s on standard FPGAs

General Description

Block diagram of PE-SE 2.1 is shown in Fig. 1.

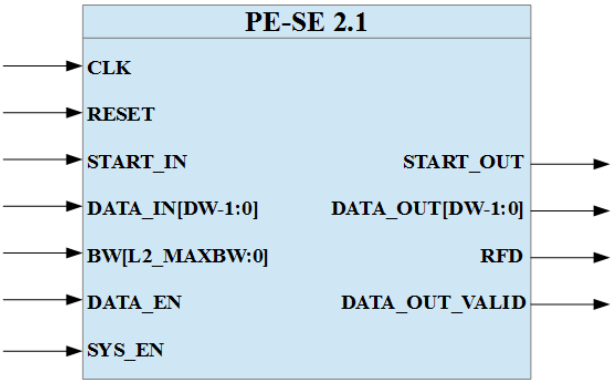

Figure 1: *Block diagram of PE-SE 2.1*

Main programmable parameters of the IP core are listed in Table 1.

Table 1: *PE-SE 2.1 Programmable Parameters*

Parameter Name	Symbol	Description
Maximum Block Width	MAX_BW	Maximum width of a code block.
Log2 (MAX_BW)	L2_MAXBW	Logarithm of MAX_BW to the base 2. Rounding up to next integer value for fractional numbers.
Code Rate	R	Number of data bits divided by BL.
Frozen Indices	FI	Frozen indices are read-in from a file.
Data Width	DW	Width of the data input/output ports.
Synthesis Platform of IP Core	SYNTHESIS_TOOL	Selection of synthesis tool, ISE or VIVADO.

The I/O ports descriptions are given in Table 2.

Table 2: *I/O Ports of PE-SE 2.1*

Pin	Sense	Port Width (bits)	Description
CLK	Input	1	All synchronous logic operations are triggered by rising edge of CLK.
RESET	Input	1	Initializes all variables and signals to their initial state synchronously.
SYS_EN	Input	1	Systematic enable, selects standard or systematic encoding operation.
DATA_IN	Input	DW	Data input (frozen and information).
START_IN	Input	1	Marks the beginning of a new data input block.
DATA_EN	Input	1	Marks valid input data.
BW	Input	L2_MAXBW	Width of a code block, takes value between 3 and MAX_BW.
DATA_OUT	Output	DW	Data output (codeword).
START_OUT	Output	1	Marks the beginning of a new data output block.
DATA_OUT_VALID	Output	1	Marks valid output data.
RFD	Output	1	Indicates the encoder is ready for new data input.

Performance

This section details the performance information of the PE-SE 2.1 for various core configurations.

Latency and Interval

Latency is the number of active clock cycles from RFD signal to the DATA_OUT_VALID signal. Interval is the number of active clock cycles between two successive RFD signals

Throughput

Throughput, maximum raw data input rate in Mbps, can be calculated as

$R * BL * (\frac{Fmax(MHz)}{INTERVAL})$.

Behavioral simulation of the PE-SE 2.1 is shown in Figure 2.

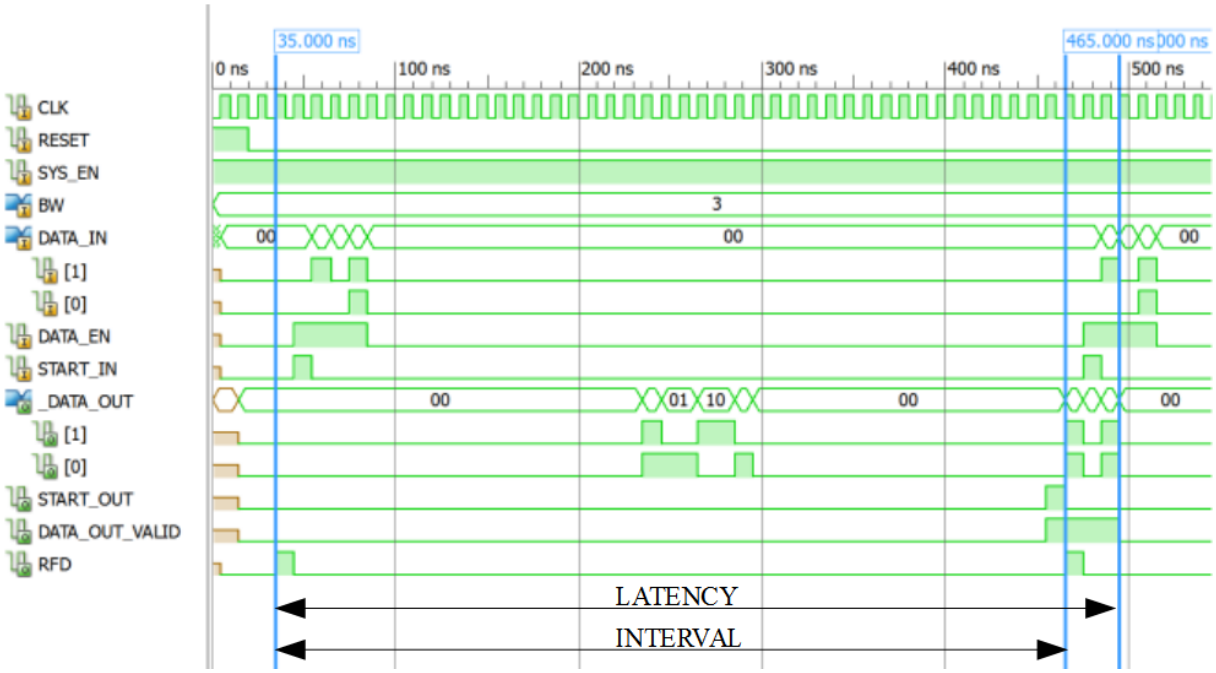

Figure 2: *Xilinx ISIM latency and interval results of PE-SE 2.1 for BL=8, DW=2, SYS_EN=1*

Latency, interval and throughput values are shown in Table 3 for selected configurations.

Table 3: *PE-SE 2.1 Performance Results*

Max Block Length (2^{MAX_BW})	Block Length	Data Width (DW)	Standard Encoding			Systematic Encoding		
			Latency (CC)	Interval (CC)	T/P (Mbps)	Latency (CC)	Interval (CC)	T/P (Mbps)
128	128	32	25	22	1354	46	43	693
256	256	32	53	46	1312	98	91	663
512	512	32	117	102	1184	218	203	595
1024	1024	32	261	230	1050	490	459	526
2048	2048	32	581	518	932	1098	1035	467
32768	32768	32	13317	12294	628	25610	24587	314
65536	65536	32	28677	26630	580	53306	53259	290

Table 4 provides formulas in order to calculate latency, interval and throughput if other configurations are preferred.

Table 4: *PE-SE 2.1 Latency, Interval and Throughput Formulas*

	Standard Encoding	Systematic Encoding
LATENCY (CC)	$3 * \left(\frac{BL}{DW}\right) + \left(\frac{BL}{DW}\right) * \log_2\left(\frac{BL}{DW}\right) + 5$	$5 * \left(\frac{BL}{DW}\right) + 2 * \left(\frac{BL}{DW}\right) * \log_2\left(\frac{BL}{DW}\right) + 10$
INTERVAL (CC)	$2 * \left(\frac{BL}{DW}\right) + \left(\frac{BL}{DW}\right) * \log_2\left(\frac{BL}{DW}\right) + 6$	$4 * \left(\frac{BL}{DW}\right) + 2 * \left(\frac{BL}{DW}\right) * \log_2\left(\frac{BL}{DW}\right) + 11$
T/P (Mbps)	$R * BL * (\frac{Fmax(MHz)}{INTERVAL})$.	$R * BL * (\frac{Fmax(MHz)}{INTERVAL})$.

Resource Utilization

Synthesis and Implementation of IP Core

PE-SE 2.1 has been synthesized with VIVADO v2013.4. The synthesis results for resource usage and maximum clock frequency are shown in Table 5.

Table 5: *PE-SE 2.1 Synthesis Results*

Max Block Length (2^{MAX_BW})	DW	FF	LUT	IOBs	BRAM	BUFG	Fmax (MHz)
128	32	186	290	77	1	1	233
256	32	197	304	77	1	1	236
512	32	210	337	77	1	1	236
1024	32	221	354	77	1	1	236
2048	32	232	374	77	1	1	236
32768	32	275	437	77	3	1	236
65536	32	286	474	77	6	1	236

PE-SE 2.1 has been implemented on Kintex-7 (*XC7K325T-2FFG900C)* Xilinx FPGA. The implementation results for resource usage are shown in Table 6.

Table 6: *PE-SE 2.1 Implementation Results*

Max Block Length (2^{MAX_BW})	**DW**	**FF**	**LUT**	**Slices**	**FF-LUT Pairs**	**IOBs**	**18k BRAMs**	**36k BRAMs**	**DSP48s**	**BUFG**
128	32	186	286	105	320	77	0	1	0	1
256	32	197	301	102	326	77	0	1	0	1
512	32	210	330	121	356	77	0	1	0	1
1024	32	221	346	121	376	77	0	1	0	1
2048	32	232	366	137	400	77	0	1	0	1
32768	32	275	416	162	488	77	0	3	0	1
65536	32	286	432	185	520	77	0	6	0	1

Further Information

For further information on product technical specifications, customization to specific applications, sales terms and pricing, please contact info@polaran.com.

PE-SE Revision History

Date	Version	Revision
03/03/15	1.0	Initial release.
09/03/15	1.1	Systematic enable pin is added.
25/11/15	2.1	Updated to version 2.1. Support for Vivado Design Suite v13.4 is added. Adaptive Block Length feature is added.